REMARKS

Claims 1-29 were pending in the Office Action. Applicants have amended Claims 1, 7-9, 11-15, 20-23, 27 and 28 and deleted Claim 29. Applicants respectfully request reconsideration and reexamination of the application.

Applicants have amended a paragraph to correct an element reference number in the text that corresponds to Figs. 8A and 8B. Specifically, "insert 710" has been changed to "insert 910" in the text. No new matter has been added. Applicants have also amended Claim 9 to correct a typographical error regarding the dependency.

Claims 7, 8, 11-15, and 20-29 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Examiner cites Claims 7, 20, and 27 as being unclear for "duplicate a physical register" and also the terms "each" and "same number" (OA, p. 3). Applicants have amended Claims 7, 20, and 27 to clarify the relationship of the register file and the register file segments, with support for the amendments found, for example, at page 10 lines 13-25 and Fig. 6 along with the corresponding text.

Examiner cites Claims 8, 21, and 28 for the scope being unclear and also for the phrase "operating equivalently" (OA, p. 3). Applicants have amended Claims 8, 21, and 28 for clarity and refer Examiner, for example, to page 10 lines 13-25 and Fig. 6 along with the corresponding text for support and a detailed description.

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Examiner cites line 8 of Claim 15 as having a typographical error (OA, p. 4). Applicants have amended the claim as suggested by Examiner by replacing "an" with "and".

Examiner notes in Claims 11 and 12 an arithmetic error (OA, p. 4). Applicants have amended Claims 11 and 12 to clarify, with support for the amendment found, for example, in Fig. 3 and the corresponding text.

Examiner cites Claim 13 and suggests the writes can not be broadcast as recited (OA, p. 4). Applicants have amended the claim for clarification with support for the amendment found, for example, at page 10 lines 13-25.

Examiner cites Claim 14 as unclear regarding bit or word lines being formed in one metal interconnect layer (OA, p. 4). Applicants have amended Claim 14 for clarity, with support found, for example, in Figs. 8A and 8B and corresponding text.

Examiner cites Claim 23 as unclear because providing a processor is not part of operating a processor (OA, p. 4). Applicants have amended the claim as suggested by Examiner.

Examiner fails to identify in the Office Action why Claims 22, 24-26, and 29 have been rejected under 35 U.S.C. § 112, second paragraph, and therefore Applicants are unable to respond regarding these claims. Applicants have cancelled Claim 29 and amended Claim 22 to correct a typographical error regarding the dependency.

Therefore, Applicants respectfully request that the rejection under 35 U.S.C. § 112, second paragraph, of Claims 7, 8, 11-15, and 20-29 be withdrawn.

Claims 1, 3-14, and 23-29 were rejected under 35 U.S.C. § 103(a) as being obvious over U.S. Patent No. 5,592,679 to Yung [herein referred to as "Yung"] in view of U.S. Patent No. 5,179,681 to Jensen [herein referred to as "Jensen"].

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Examiner admits that Yung does not disclose whether the global register and the local register sets are partitioned from a register file and cites Jensen as disclosing partitioning of registers (OA, p. 2). From this Examiner reasons that because "both references are directed toward associating global register set and local register set to a functional unit, it would have been obvious to a person of ordinary skill in the art to implement a plurality of global register sets and local register sets by partitioning a register file as taught by Jensen in the multi functional units processing system of Yung if a single large register file is available rather than a plurality of smaller registers."

Applicants respectfully disagree that Yung or Jensen, alone or in combination, disclose all elements of the present invention. Neither reference alone or in combination discloses "a register file that is divided into a plurality of register file segments, ones of the plurality of register file segments being coupled to and associated with ones of the plurality of functional units, the register file segments being partitioned into global registers and local registers" as recited in Claim 1 or "the plurality of register file segments being coupled and associated to ones of the plurality of functional units" and "partitioning the register file segments into global registers and local registers" as recited in Claim 23.

Yung discloses in Fig. 2 a DDF processor 200 that "includes an instruction cache memory 210, a plurality of prefetch buffers 221, 222, ... 229, a global instruction scheduler 230, a plurality of execution pipes 241, 242,... 249, one or more inter-pipe bypass(es) 251, ... 259, an arbiter 260, and a global register file/memory 290. Each instruction pipe includes its own ... temporary local register buffer" (col. 4, lns. 59-67). Each execution unit within an execution pipe has only a local register buffer and must utilize an arbiter 260 via an inter-pipe operand request (col. 6, lns. 45-50) to request access to global register file 290 (col. 7, lns. 4-11). Thus, combining Jensen with the architecture disclosed in Yung (e.g., arbiter, inter-pipe

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bypasses, etc.) would still fail to disclose aspects of the invention, as noted in the claim language above, and there would also be no motivation to do so.

Furthermore, Yung teaches away from certain embodiments of the present invention by the following.

> The hierarchical register file system which includes global register file 290 and multiple local register buffers 241d, 242d, ... 249d is advantageous over the prior art for the following reasons. A single centralized register file is not ideal because interconnecting the large fast global memory to a large number of execution units is prohibitively expansive in silicon area and requires extremely complex circuitry with many I/O ports. This expansion increases exponentially as the size of the global memory and/or the number of execution units increase. (col. 6, lns. 18-28) (emphasis added)

Furthermore, neither Yung nor Jensen, alone or in combination, teach or suggest that "the number of global registers and the number of local registers are programmably configurable" as recited in amended Claim 1 or "programmably partitioning the register file so that the number of the global registers and the number of the local registers are selectable and variable" as recited in amended Claim 23.

For the dependent claims, Examiner stated that "given the configuration of the processing system and the register file, it would have been obvious to a person of ordinary skill in the art to use an address space dependent on the configuration for addressing the partitioned register file such that the local register sets and the global register sets can be accessed by the functional units because otherwise it would not work" (OA, p. 2). Applicants respectfully disagree and request that Examiner cite a prior art reference supporting this opinion for the dependent claim limitations so that Applicants can respond accordingly.

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Therefore, Applicants respectfully submit that Claims 1 and 23 patentably distinguish over Yung in view of Jensen and that dependent Claims 3-14 and 24-28 (Claim 29 has been cancelled) are also distinguishable for at least the same reasons as for corresponding independent Claims 1 and 23. Therefore, Applicants respectfully request that the rejection under 35 U.S.C. § 103(a) of Claims 1, 3-14, and 23-29 be withdrawn.

Claims 2 and 15-22 were rejected under 35 U.S.C. § 103(a) as being obvious over Yung and Jensen and in view of U.S. Patent No. 6,023,757 to Nishimoto et al [herein referred to as "Nishimoto"].

Examiner cites Nishimoto for disclosing VLIW instructions. However, Nishimoto fails to cure the deficiencies noted above for Yung and Jensen for Claim 1, which Claim 2 depends upon. For Claim 15, neither Yung, Jensen, or Nishimoto, alone or in combination, teach or suggest for reasons discussed above, "the register file segments including a plurality of registers that are partitioned into global registers and local registers, the global registers being accessible by the plurality of functional units, the local registers in one of the register file segments being accessible by the functional unit associated with the register file segment" as recited in Claim 15.

Therefore, Applicants respectfully submit that Claims 1 and 15 patentably distinguish over Yung and Jensen in view of Nishimoto and that dependent Claims 2 and 16-22 are also distinguishable for at least the same reasons as for corresponding independent Claims 1 and 15. Therefore, Applicants respectfully request that the rejection under 35 U.S.C. § 103(a) of Claims 2 and 15-22 be withdrawn.

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Accordingly, Applicants respectfully submit that Claims 1-28 are in proper form for allowance. Reconsideration and withdrawal of the rejections are respectfully requested and a

timely Notice of Allowance is solicited. If there are any questions regarding any aspect of the application, please call the undersigned at (949) 718-5221.

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Respectfully submitted,

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ATTACHMENT A

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the following, insertions are underlined and deletions are enclosed in brackets.

The paragraph starting on page 20 line 27 and ending on page 21 line 14, is amended as follows:

The register file **216** includes a decoder, as is shown in **FIGURE 6**, for each of the sixteen read and write ports. The register file **216** includes a memory array **940** that is partially shown in the insert **910** [710] illustrated in **FIGURE 8B** and includes a plurality of word lines **944** and bit lines **946**. The word lines **944** and bit lines **946** are simply a set of wires that connect transistors (not shown) within the memory array **940**. The word lines **944** select registers so that a particular word line selects a register of the register file **216**. The bit lines **946** are a second set of wires that connect the transistors in the memory array **940**. Typically, the word lines **944** and bit lines **946** are laid out at right angles. In the illustrative embodiment, the word lines **944** and the bit lines **946** are constructed of metal laid out in different planes such as a metal 2 layer for the word lines **944** and a metal 3 layer for the bit lines **946**. In other embodiments, bit lines and word lines may be constructed of other materials, such as polysilicon, or can reside at different levels than are described in the illustrative embodiment, that are known in the art of semiconductor manufacture. In the illustrative example, the word lines **944** are separated by a distance of about 1μm and the bit lines **946** are separated by approximately 1μm. Other circuit dimensions may be constructed for various processes. The illustrative example shows one bit line per port, other embodiments may use multiple bit lines per port.

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The claims are amended as shown below.

1. A processor comprising:

a plurality of functional units; and

a register file that is divided into a plurality of register file segments, ones of the plurality of register file segments being coupled to and associated with ones of the plurality of functional units, the register file segments being partitioned into global registers and local registers, the global registers that are accessible by the plurality of functional units, the local registers being accessible by the functional unit associated with the register file segment containing the local registers, wherein the number of global registers and the number of local registers are programmably configurable.

7. A processor according to Claim 1 wherein:

the register file includes [N physical registers and is duplicated into] M of the register file segments, with each of the M register file segments having N physical registers, the register file segments having a reduced number of read and/or write ports in comparison to an undivided [nonduplicated] register file[, but each having the same number of physical registers].

8. A processor according to Claim 7 wherein:

the register file segments are partitioned into N_G global and N_L local register files where N_G plus N_L is equal to N, the register file [operating equivalently to a register file] having $N_G + (M * N_L)$ total registers available for the M functional units, the number of address bits for addressing the $N_G + (M * N_L)$ total registers being equal to the number of bits B that are used to address $N = 2^B$ registers[, the local registers for ones of the M register file segments are addressed using the same B-bit values].

9. A processor according to Claim 8 [6] wherein:

partitioning of the register file is programmable so that the number N_G of global registers and number N_L of local registers is selectable and variable.

11. A processor according to Claim 10 wherein:

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the storage array structure is a [sixteen] multi-port structure [with twelve read ports and five write ports]; and

the plurality of storage array storages includes four storage array storages each having three read ports and five write ports.

12. A processor according to Claim 10 wherein:

the storage array structure is a [sixteen] multi-port structure [with twelve read ports and four write ports]; and

the plurality of storage array storages includes four storage array storages each having three read ports and four write ports.

13. A processor according to Claim 10 wherein:

the writes for the global registers are fully broadcast so that all of the storage array storages are held coherent.

14. A processor according to Claim 10 wherein:

storage array storages include storage cells having a plurality of word lines and a plurality of bit lines, the word lines being formed in one metal [interconnect] layer, the bits lines being formed in a second metal [interconnect] layer.

15. A processor comprising:

a decoder for decoding a very long instruction word including a plurality of subinstructions, the subinstructions being allocated into positions of the instruction word;

a register file coupled to the decoder and divided into a plurality of register file segments; and

a plurality of functional units, ones of the plurality of functional units being coupled to and associated with respective ones of the register file segments, ones of the plurality of subinstructions being executable upon respective ones of the plurality of functional units, operating upon operands accessible to the register file segment associated with the functional unit of the plurality of functional units, the register file segments including a plurality of registers that are partitioned into global registers and local registers, the global registers being accessible by the plurality of functional units, the local registers in one of the

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register file segments being accessible by the functional unit associated with the register file segment.

20. A processor according to Claim 15 wherein:

the register file includes [N physical registers and is duplicated into] M of the register file segments, with each of the M register file segments having N physical registers, the register file segments having a reduced number of read and/or write ports in comparison to an undivided [nonduplicated] register file[, but each having the same number of physical registers].

21. A processor according to Claim 20 wherein:

the register file segments are partitioned into N_G global and N_L local register files where N_G plus N_L is equal to N, the register file [operating equivalently to a register file] having $N_G + (M * N_L)$ total registers available for the M functional units, the number of address bits for addressing the $N_G + (M * N_L)$ total registers being equal to the number of bits B that are used to address $N = 2^B$ registers[, the local registers for ones of the M register file segments are addressed using the same B-bit values].

22. A processor according to Claim 21 [20] wherein:

partitioning of the register file is programmable so that the number N_G of global registers and number N_L of local registers is selectable and variable.

23. A method of operating a processor, the processor including a plurality of functional units and a register file divided into a plurality of register file segments, the plurality of register file segments being coupled and associated to ones of the plurality of functional units, comprising:

[providing a processor including a plurality of functional units and a register file divided into a plurality of register file segments, the plurality of register file segments being coupled and associated to ones of the plurality of functional units;]

partitioning the register file segments into global registers and local registers;

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operating the plurality of functional units;

accessing the global registers by the plurality of functional units; [and]

accessing the local registers by the functional unit associated with the register file segment containing the local registers; and

programmably partitioning the register file so that the number of the global registers and the number of the local registers are selectable and variable. .

27. A method according to Claim 23, wherein the register file includes M of the register file segments, with each of the M register file segments having N physical registers, [further comprising:

including N physical registers in the register file;

duplicated the physical registers into M register file segments,] the register file segments having a reduced number of read and/or write ports in comparison to an undivided [nonduplicated] register file[, but each having the same number of physical registers].

28. A method according to Claim 27 further comprising:

partitioning the register file segments into N_G global and N_L local register files where N_G plus N_L is equal to N; and

operating the register file [equivalently to a register file] having $N_G + (M * N_L)$ total registers available for the M functional units, the number of address bits for addressing the $N_G + (M * N_L)$ total registers being equal to the number of bits B that are used to address $N = 2^B$ registers[; and

addressing the local registers for ones of the M register file segments using the same B-bit values].

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